UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/942,812	08/29/2001	Ken Shoemaker	2207/10127	8429

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EXAMINER
MEONSKE, TONIA L

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)
Office Action Summary		09/942,812	SHOEMAKER, KEN
		Examiner	Art Unit	
		Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2005*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-8* is/are allowed.

6)☒ Claim(s) *9-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2.   Claims 9-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Simultaneous

Multithreading: A Platform for Next-Generation Processors, Susan Eggers, et al. (hereinafter

referred to as Eggers et al.), cited by examiner on July 12, 2004.

3.   Referring to claim 9, Eggers et al. have taught a method for switching threads in a multi-

threading processor, comprising:

        a.   fetching a first active thread and a active second thread (Page 14, Instruction

fetching section, Page 13, right hand column, first full paragraph, Each cycle only instructions

from two threads are fetched in the pipeline, however threads from up to eight contexts are

simultaneously executed throughout the entire pipeline. When a thread has the fewest number of

instructions executing in the pipeline, that thread is chosen for instruction fetching by using an

Icount feedback to avoid thread starvation. When a thread has at least one instruction in the

pipeline, then the thread is active. Therefore, since Eggers has taught instructions from up to

eight thread contexts simultaneously executing in the pipeline, then Eggers has taught up to eight

active threads. Therefore when Eggers fetches two threads of eight active threads, Eggers is

fetching a first active thread and a second active thread as claimed.);

b.   detecting a stalling event in said first active thread (Page 14, A cache miss is a long-latency event, or stalling event, for a thread. When an active thread executing in the pipeline experiences a cache miss, instructions in the thread after the cache miss, must wait until data is retrieved from a slower memory before executing. Instead of waiting on the thread to completely service the cache miss, Eggers has taught selecting instructions from two other threads not incurring instruction cache misses. Since Eggers has taught selecting two different threads from those not already incurring instruction cache misses, then Egers must be detecting the stalling event as claimed.); and

c.   switching said first active thread with a third thread, if said third thread is ready to execute (Page 14, right hand column, 3rd full paragraph, also see the first paragraph of section "2.8fetching", When the first active thread experiences a cache miss, then a thread that is not executing instructions, or a third thread, will be chosen for fetching.).

4.   Referring to claim 10, Eggers et al. have taught a method for switching threads as recited in claim 9, as described above, and further comprising executing said third thread and said second active thread (page 14, Instructions in the pipeline are instructions that are executing. When an instruction in the third thread is fetched, as described above in claim 9, the third thread begins executing. When an instruction from the second active thread is fetched, as described above in claim 9, then the second active thread begins executing.).

5.   Referring to claim 11, Eggers et al. have taught a method for switching threads as recited in claim 9, as described above, and further comprising detecting a stalling event in the second active thread (Page 14, A cache miss is a long-latency event, or stalling event, for a thread. When an active thread executing in the pipeline experiences a cache miss, instructions in the

thread after the cache miss, must wait until data is retrieved from a slower memory before executing. Instead of waiting on the thread to completely service the cache miss, Eggers has taught selecting instructions from two other threads not incurring instruction cache misses. Since Eggers has taught selecting two different threads from those not already incurring instruction cache misses, then Egers must be detecting the stalling event as claimed.).

6.   Referring to claim 12, Eggers et al. have taught a method for switching threads as recited in claim 11, as described above, and further comprising switching said second active thread with a fourth thread, if the fourth thread is ready to execute (Page 14, right hand column, 3rd full paragraph, also see the first paragraph of section "2.8fetching", When the second active thread experiences a cache miss, then a thread that is not executing an instruction, or a fourth thread, will be chosen for fetching.).

7.   Referring to claim 13, Eggers et al. have taught a method for switching threads as recited in claim 12, as described above, and further comprising executing the third thread and the fourth thread (Page 14, Instructions in the pipeline are instructions that are executing. When an instruction in the third thread is fetched, as described above in the rejection to claim 9, the third thread begins executing. When an instruction from the fourth thread is fetched, as described above in the rejection to claim 12, then the fourth thread begins executing.).

8.   Referring to claim 14, Eggers et al. have taught a method for switching threads as recited in claim 9, as described above, and further comprising executing the second active thread, if the first inactive thread is not ready to execute (page 14, Threads that fetch instructions into the pipeline are executed regardless of whether other threads are ready to execute. Therefore, if the

third thread is not ready to execute, then the second active thread continues executing the fetched

instructions in the pipeline.).

9.   Claim 15 does not recite limitations above the claimed invention set forth in claim 9 and

is therefore rejected for the same reasons set forth in the rejection of claim 9 above.

10.   Claim 16 does not recite limitations above the claimed invention set forth in claim 10 and

is therefore rejected for the same reasons set forth in the rejection of claim 10 above.

11.   Claim 17 does not recite limitations above the claimed invention set forth in claim 11 and

is therefore rejected for the same reasons set forth in the rejection of claim 11 above.

12.   Claim 18 does not recite limitations above the claimed invention set forth in claim 12 and

is therefore rejected for the same reasons set forth in the rejection of claim 12 above.

13.   Claim 19 does not recite limitations above the claimed invention set forth in claim 13 and

is therefore rejected for the same reasons set forth in the rejection of claim 13 above.

14.   Claim 20 does not recite limitations above the claimed invention set forth in claim 14 and

is therefore rejected for the same reasons set forth in the rejection of claim 14 above.

Allowable Subject Matter

15.   Claims 1-8 are allowed.

16.   The following is a statement of reasons for the indication of allowable subject matter:

a.   Claim 1, lines 7-9 state "a register file coupled to said execution unit, wherein

said register file is to switch one of said active thread and said second active thread with a

first inactive thread". The prior art of record has taught the claimed first and second fetch

units, the multi-thread scheduler, and the execution unit. The prior art has not taught the

claimed register file switching one thread with another thread in combination with the

separate first and second fetch units, the multi-thread scheduler and the execution unit

(See citation U, page 334, section 2.4.7 and citation V, page 2, section 3). The prior art

simultaneous multithreaded (SMT) processors of claim 1, excluding the claimed register

file in lines 7-9, normally have several register files so that each thread has its own

register file. Having the threads with separate register files has been necessary for fast

context switching required in SMT processors. With the separate register files, data is

not switched in an out of a single register file, as in the instant claimed invention.

Furthermore it would not have been obvious to one of ordinary skill in the art at the time

of the invention to have the simultaneous multithreaded process of claim 1 have "a

register file coupled to said execution unit, wherein said register file is to switch one of

said active thread and said second active thread with a first inactive thread" as this would

have created more thread switching overhead and decrease instruction throughput.

Response to Arguments

17.   Applicant's arguments with respect to claims 9-20 have been considered but are moot in

view of the newly explained ground(s) of rejection above.

Conclusion

18.   Applicant's amendment necessitated the new ground(s) of rejection presented in this

Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

19.   A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this

final action.

20.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170.

The examiner can normally be reached on Monday-Friday, with every other Friday off.

21.   If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

22.   Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

HENRY W. H. TSAI
PRIMARY EXAMINER

1/20/06